What Is Claimed Is:

1. A semiconductor integrated circuit device having a plurality of circuit elements and a plurality of wires connecting the circuit elements, comprising:

an orthogonal wire having a first minimum wire width, which is formed in a first wiring layer and extends horizontally or vertically;

a diagonal wire having a second minimum wire width which is substantially equal to said first minimum wire width, which is formed in a second wiring layer which differs from said first wiring layer and extending in a diagonal direction in relation to said orthogonal wire; and

a via having a size which is no greater than said first or second minimum wire width, which is formed at point at which said orthogonal wire and said diagonal wire overlap so as to connect said orthogonal wire and said diagonal wire,

wherein one of said diagonal wire and said orthogonal wire includes an enlarged wire width region in a position at which said via is formed, the wire width of said enlarged wire width region being enlarged beyond said first or second minimum wire width.

2. The semiconductor integrated circuit according to claim 1, wherein said via has a rectangular form in which the length of one edge is shorter than said first or second

minimum wire width, the rectangle is provoded in the same direction as one of said diagonal wire and said orthogonal wire, and the other of said diagonal wire and said orthogonal wire includes said enlarged wire width region.

3. A wiring layout method for a semiconductor integrated circuit device having a plurality of circuit elements and a plurality of wires connecting the circuit elements, comprising :

generating data for an orthogonal wire having a first minimum wire width, which is formed in a first wiring layer and extends horizontally or vertically;

generating data for a diagonal wire having a second minimum wire width which is substantially equal to said first minimum wire width, formed in a second wiring layer which differs from said first wiring layer and extending in a diagonal direction in relation to said orthogonal wire; and

generating data for a via figure at point at which said orthogonal wire and said diagonal wire overlap, said via figure being constituted by a via having a size which is no greater than said first or second minimum wire width, a first via cushion conductive layer which is larger than said via and formed in said first wiring layer, and a second via cushion conductive layer which is larger than said via and formed in said second wiring layer,

wherein said first or second via cushion

conductive layer is larger than the minimum wire width of said orthogonal wire or said diagonal wire.

4. The layout method for a semiconductor device according to claim 3, wherein said via has a first rectangular form in which a length of one edge is shorter than said first minimum wire width, and

said first and second via cushion conductive layers have a second rectangular form which is larger than said first rectangular form, the second rectangular form is provided in the same direction as one of said diagonal wire and said orthogonal wire, and the other of said diagonal wire and said orthogonal wire includes an enlarged wire width region having a wire width which is enlarged beyond said first or second minimum wire width by said first or second via cushion conductive layer.

5. The layout method for a semiconductor device according to claim 3, wherein said via has a first rectangular form in which a length of one edge is shorter than said first minimum wire width, and

said first and second via cushion conductive layers has a second rectangular form which is larger than said first rectangular form, the second rectangular form is provoded in the same direction as said orthogonal wire, and said diagonal wire includes an enlarged wire width region having a wire width which is enlarged beyond said

second minimum wire width by said second via cushion conductive layer.

6. A semiconductor integrated circuit device having a plurality of circuit elements and a plurality of wires connecting the circuit elements, comprising:

orthogonal wires formed on a standard grid which has a pitch P and extends in a horizontal or vertical direction, and disposed at intervals of at least said pitch P; and

diagonal wires inclined by 45° or 135° in relation to said orthogonal wires,

wherein said diagonal wires include a first diagonal wire formed on a grid point of said standard grid and a second diagonal wire formed on a 1/2 grid point at which said standard grid intersects a 1/2 grid which is displaced from said standard grid by P/2, said first and second diagonal wires being disposed at intervals of at least $(1.5/\sqrt{2})\times P$ in relation to said pitch P.

7. The semiconductor integrated circuit device according to claim 6, wherein said orthogonal wires are formed on said 1/2 grid in addition to said standard grid.

8. The semiconductor integrated circuit device according to claim 6, wherein the minimum wire width of said diagonal wire is substantially same as the minimum

wire width of said orthogonal wire.

9. The semiconductor integrated circuit device according to claim 6, wherein the positions on said orthogonal wire at which the orthogonal wire intersects said first and second diagonal wires have a minimum pitch of 1.5P.

10. The semiconductor integrated circuit device according to claim 6, wherein an orthogonal wire which is adjacent to a predetermined orthogonal wire intersects a diagonal wire which is adjacent to a predetermined diagonal wire at a position which is located a knight's move from the intersection position of said predetermined orthogonal wire and said predetermined diagonal wire.

11. A wiring layout method for a semiconductor integrated circuit having a plurality of circuit elements and a plurality of wires connecting the circuit elements, comprising :

generating data, in a first wiring layer, for orthogonal wires disposed on a standard grid, which has a pitch P and extends in a horizontal or vertical direction, at intervals of at least said pitch P; and

generating data, in a second wiring layer, which differs from said first wiring layer, for diagonal wires inclined by 45° or 135° in relation to said orthogonal wires,

said data for diagonal wires including data for a first diagonal wire formed on a grid point of said standard grid, and data for a second diagonal wire formed on a 1/2 grid point at which said standard grid intersects a 1/2 grid which is displaced from said standard grid by P/2,

wherein said first and second diagonal wires are disposed at intervals of at least $(1.5/\sqrt{2}) \times P$ in relation to said pitch P.

12. The wiring layout method for a semiconductor integrated circuit according to claim 11, wherein data for orthogonal wires formed on said 1/2 grid in addition to said standard grid are generated in said step of generating the data for orthogonal wire.

13. The wiring layout method for a semiconductor integrated circuit according to claim 11, wherein said data for orthogonal wire have a first minimum wire width, and said data for diagonal wire have a second minimum wire width which is substantially equal to said first minimum wire width.

14. The wiring layout method for a semiconductor device according to claim 13, further comprising generating data for a via figure at a point at which said orthogonal wire and said diagonal wire overlap, said via figure being constituted by a via having a size which is

no greater than said first or second wire width, a first via cushion conductive layer which is larger than said via and formed in said first wiring layer, and a second via cushion conductive layer which is larger than said via and formed in said second wiring layer,

wherein said first or second via cushion conductive layer is larger than the minimum wire width of said orthogonal wire or said diagonal wire.

15. A semiconductor device wiring layout program for causing a computer to execute a wiring layout procedure for a semiconductor integrated circuit having a plurality of circuit elements and a plurality of wires connecting the circuit elements, said wiring layout procedure comprising :

generating data for an orthogonal wire having a first minimum wire width, which is formed in a first wiring layer and extends horizontally or vertically;

generating data for a diagonal wire having a second minimum wire width which is substantially qual to said first minimum wire width, formed in a second wiring layer which differs from said first wiring layer and extending in a diagonal direction in relation to said orthogonal wire; and

generating data for a via figure at point at which said orthogonal wire and said diagonal wire overlap, said via figure being constituted by a via having a size

which is no greater than said first or second minimum wire width, a first via cushion conductive layer which is larger than said via and formed in said first wiring layer, and a second via cushion conductive layer which is larger than said via and formed in said second wiring layer,

wherein said first or second via cushion conductive layer is larger than the minimum wire width of said orthogonal wire or said diagonal wire.

16. A semiconductor integrated circuit wiring layout program for causing a computer to execute a wiring layout procedure for a semiconductor integrated circuit having a plurality of circuit elements and a plurality of wires connecting the circuit elements, said wiring layout procedure comprising :

generating data, in a first wiring layer, for orthogonal wires disposed on a standard grid, which has a pitch P and extends in a horizontal or vertical direction, at intervals of at least said pitch P; and

generating data, in a second wiring layer, which differs from said first wiring layer, for diagonal wires inclined by 45° or 135° in relation to said orthogonal wires, said data for diagonal wires including data for a first diagonal wire formed on a grid point of said standard grid, and data for a second diagonal wire formed on a 1/2 grid point at which said standard grid intersects a 1/2 grid which is displaced from said standard grid by P/2,

wherein said first and second diagonal wires are disposed at intervals of at least $(1.5/\sqrt{2}) \times P$ in relation to said pitch P.